UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/911,495	07/25/2001	Barbara F. Barenburg	211810US99	4424

22850 7590 06/05/2003

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
COLEMAN, WILLIAM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 06/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/911,495	Applicant(s) BARENBURG ET AL.
	Examiner W. David Coleman	Art Unit 2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10-20 and 22-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10-20 and 22-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *12* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 27, 2003 has been entered.

Claim Rejections - 35 USC § 102

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
>
> (f) he did not himself invent the subject matter sought to be patented.

2. Claims 1-8, 10-20 and 22-24 are rejected under 35 U.S.C. 102(f) because the applicant did not invent the claimed subject matter. Ramdani et al., U.S. Patent 6,392,257 B1 states, "High quality epitaxial layers of compound semiconductor materials can be grown overlying large silicon wafers by first growing an accommodating buffer layer on a silicon wafer. The accommodating buffer layer is a layer of monocrystalline oxide spaced apart from the silicon wafer by an amorphous interface layer of silicon oxide. The amorphous interface layer dissipates strain and permits the growth of a high quality monocrystalline oxide accommodating buffer layer. The accommodating buffer layer is lattice matched to both the underlying silicon wafer and the overlying monocrystalline compound semiconductor layer. Any lattice mismatch between the accommodating buffer layer and the underlying silicon substrate is taken care of by

the amorphous interface layer (see Abstract) Ramdani further discloses an optical interconnect waveguide.

3. Claims 1-8 and 10-20 and 22-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Lach et al., U.S. Patent 6,498,358 B1.

See **FIGS. 1-49** where Lach teaches the claimed inventions.

Pertaining to claim 1, Lach teaches a semiconductor structure comprising:

a monocrystalline silicon substrate **52** (see **FIG. 24**);

an amorphous oxide material **62** overlying the monocrystalline silicon substrate **52**;

a monocrystalline perovskite oxide material **65** overlying the amorphous oxide material **62**;

a monocrystalline compound semiconductor material **66** overlying, the monocrystalline perovskite oxide material; and

an arrayed wavelength grating device overlying the monocrystalline silicon substrate, wherein the arrayed wavelength grating device comprises a plurality of electro-optical waveguides formed within the monocrystalline compound semiconductor layer, each waveguide of the plurality of electro-optical waveguides carrying an optical signal of a distinct wavelength, and a first electrode formed in the monocrystalline compound semiconductor layer and above the plurality of electro-optical waveguides, the first electrode operable to provide a distinct phase shift to each waveguide of the plurality of electro-optical waveguides in response to an application of voltage to the first electrode (see columns 25-29 where Lach teaches individual electrochromic sections **4012-4026** for the arrayed wavelength gratings).

4. Pertaining to claim 10, Lach teaches the semiconductor structure of claim 1, wherein: the arrayed wavelength grating device further comprises a planar waveguide region in optical communication with the plurality of electro-optical waveguides, and a second electrode formed in the monocrystalline compound semiconductor layer and above the planar waveguide region, the second electrode operable to tune a temperature sensitivity of the plurality of electro-optical waveguides.

5. Pertaining to claim 11, Lach teaches the semiconductor structure of claim 1, wherein: the arrayed wavelength grating device further comprises a planar waveguide region in optical communication with the plurality of electro-optical waveguides, and a second electrode formed in the monocyrstalline compound semiconductor layer and above the planar waveguide region, the second electrode operable to tune a polarization-dependent wavelength of the plurality of electro-optical waveguides.

6. Pertaining to claim 12, Lach teaches the semiconductor structure of claim 1, wherein: the arrayed wavelength grating device further comprises:
a planar waveguide region in optical communication with the plurality of electro-optical waveguides, and a second electrode formed in the monocyrstalline compound semiconductor layer and above the planar waveguide region, the second electrode operable to tune a channel wavelength offset of the plurality of electro-optical waveguides.

7. Pertaining to claim 13, Lach teaches a process for fabricating a semiconductor structure comprising: providing a monocrystalline silicon substrate; depositing a monocrystalline perovskite oxide film overlying the monocrystalline silicon substrate, the film having a thickness less than a thickness of the material that would result in strain-induced defects; forming an amorphous oxide interface layer containing at least silicon and oxygen at an interface between the monocrystalline perovskite oxide film and the monocrystalline silicon substrate; epitaxially forming a monocrystalline compound semiconductor layer overlying the monocrystalline perovskite oxide film; and forming an arrayed wavelength grating device overlying the monocrystalline silicon substrate, wherein the arrayed wavelength grating device comprises a plurality of electro-optical waveguides formed within the monocrystalline compound semiconductor layer, each waveguide of the plurality of el electro-optical waveguides carrying an optical signal of a distinct wavelength, and a first electrode formed in the monocyrstalline compound semiconductor layer and above the plurality of electro-optical waveguides, the first electrode operable to provide a distinct phase shift to each waveguide of the plurality of electro-optical waveguides in response to an application of voltage to the first electrode.

8. Pertaining to claim 22, Lach teaches the process of claim 13, wherein: the arrayed wavelength grating device further comprises a planar waveguide region in optical communication with the plurality of electro-optical waveguides, and a second electrode formed in the monocyrstalline compound semiconductor layer and above the planar waveguide region,

the second electrode operable to tune a temperature sensitivity of the plurality of electro-optical waveguides.

9. Pertaining to claim 23, Lach teaches the process of claim 13, wherein: the arrayed wavelength grating device further comprises a planar waveguide region in optical communication with the plurality of electro-optical waveguides, and a second electrode formed in the monocyrstalline compound semiconductor layer and above the planar waveguide region, the second electrode operable to tune a polarization dependent wavelength of the plurality of electro-optical waveguides.

10. Pertaining to claim 24, Lach teaches the process of claim 13, wherein:

the arrayed wavelength grating device further comprises a planar waveguide region in optical communication with the plurality of electro-optical waveguides, and a second electrode formed in the monocyrstalline compound semiconductor layer and above the planar waveguide region, the second electrode operable to tune a channel wavelength offset of the plurality of electro-optical waveguides.

11. Pertaining to claim 2, Lach teaches the semiconductor structure of claim 1, wherein:

the arrayed wavelength grating device functions as a multiplexer.

12. Pertaining to claim 3, Lach teaches the semiconductor structure of claim 1, wherein:

the arrayed wavelength grating device functions as a demultiplexer.

13. Pertaining to claim 4, Lach teaches the semiconductor structure of claim 1, wherein:

the arrayed wavelength grating device functions as a router.

14. Pertaining to claim 5, Lach teaches the semiconductor structure of claim 1, wherein: the arrayed wavelength grating device functions as a switch.

15. Pertaining to claim 6, Lach teaches the semiconductor structure of claim 1, wherein: a temperature sensitivity of the arrayed wavelength grating device is tunable.

16. Pertaining to claim 7, Lach teaches the semiconductor structure of claim 1, wherein: a polarization dependent wavelength of the arrayed wavelength grating device is tunable.

17. Pertaining to claim 8, Lach teaches the semiconductor structure of claim 1, wherein: a channel wavelength offset of the arrayed wavelength grating device is tunable.

18. Pertaining to claim 14, Lach teaches the process of claim 13, wherein: the arrayed wavelength grating device functions as a multiplexer.

19. Pertaining to claim 15, Lach teaches the process of claim 13, wherein: the arrayed wavelength grating device functions as a demultiplexer.

20. Pertaining to claim 16, Lach teaches the process of claim 13, wherein: the arrayed wavelength grating device functions as a router.

21. Pertaining to claim 17, Lach teaches the process of claim 13, wherein:

the arrayed wavelength grating device functions as a switch.

22. Pertaining to claim 18, Lach teaches the process of claim 13, wherein: a temperature sensitivity of the arrayed wavelength grating device is tunable.

23. Pertaining to claim 19, Lach teaches the process of claim 13, wherein:

a polarization dependent wavelength of the arrayed wavelength grating device is tunable.

24. Pertaining to claim 20, Lach teaches the process of claim 13, wherein:

a channel wavelength offset of the arrayed wavelength grating device is tunable.

Conclusion

25. The Examiner will consider entry of a terminal disclaimer that place all of the claims in condition for allowance, even if submitted after prosecution is closed.

26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 703-305-0004. The examiner can normally be reached on 9:00 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the

organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7721 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

W. David Coleman
Primary Examiner
Art Unit 2823

WDC
May 30, 2003